

FIG.1

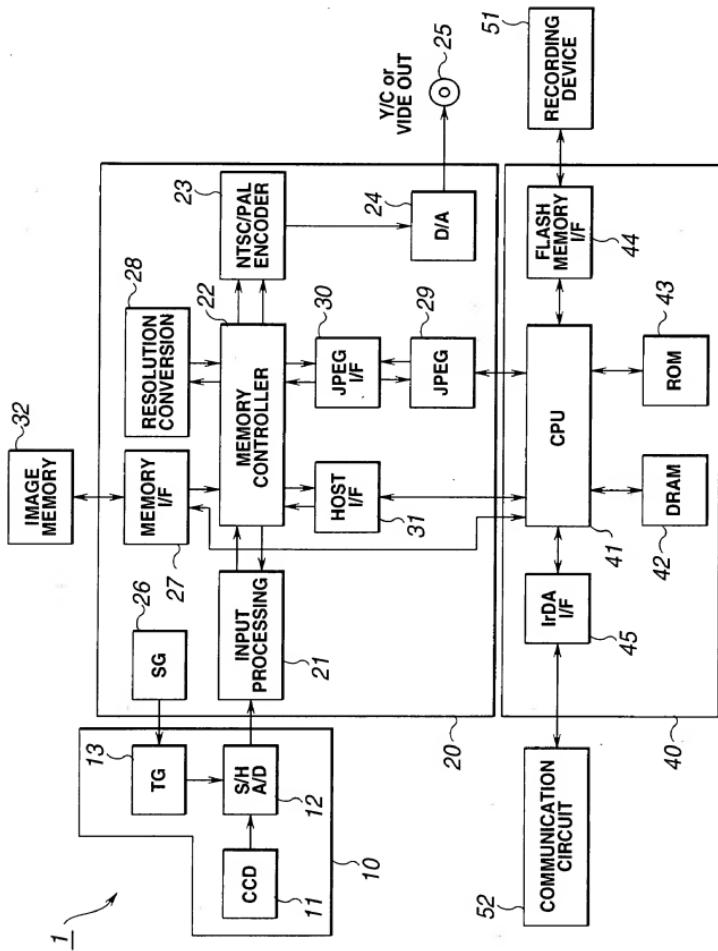


FIG.2

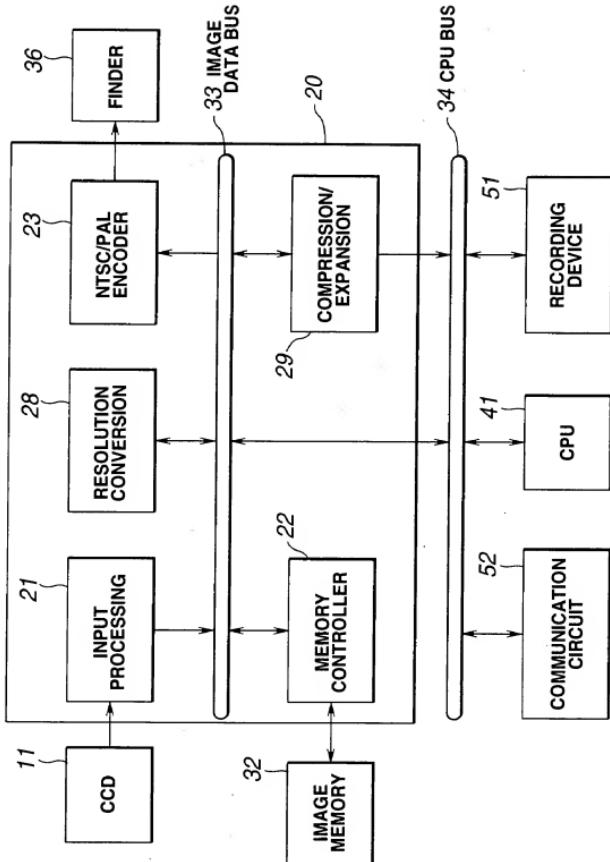


FIG.3

APPROVED	O.G. FIG.
BY	CLASS
DRAFTSMAN	SUBCLASS

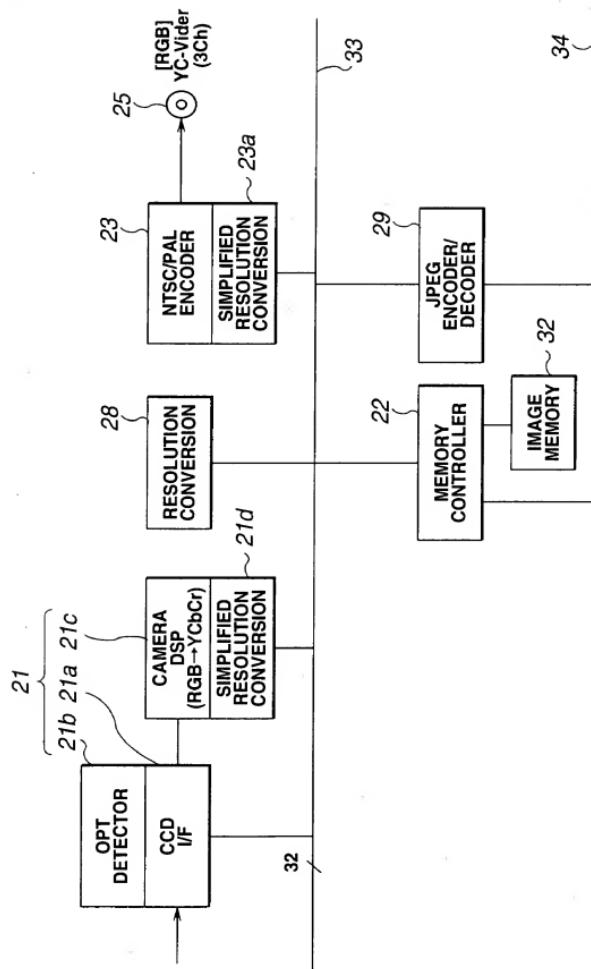


FIG.4

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

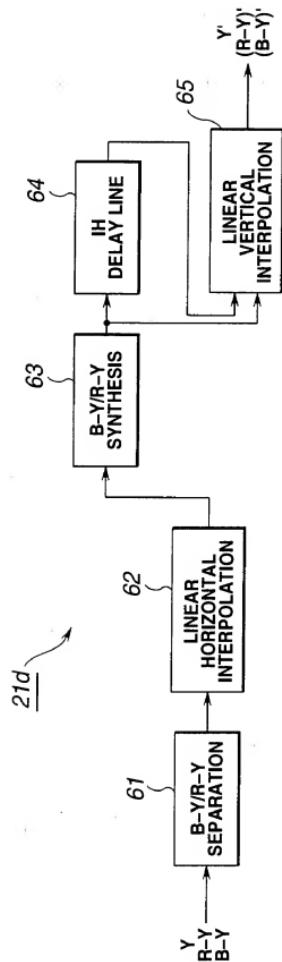


FIG.5

APPROVED BY DRAFTSMAN	O.G. FIG.	
	CLASS	SUBCLASS

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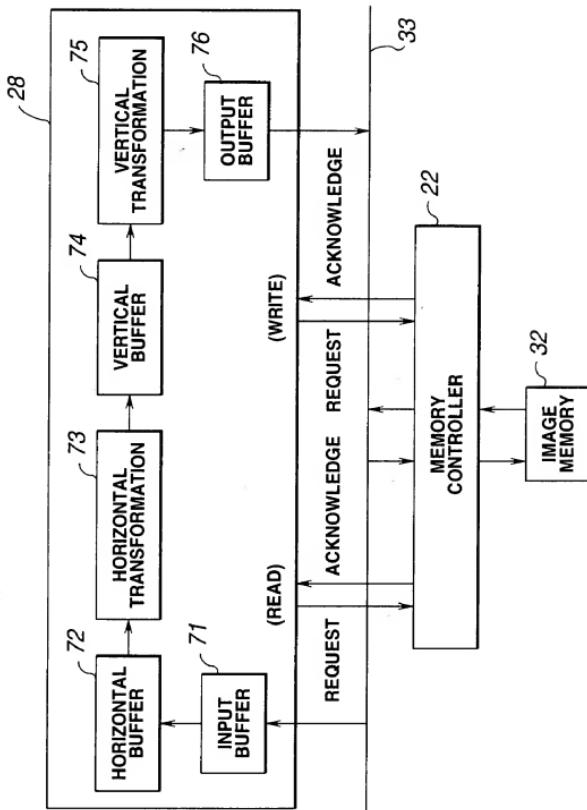


FIG. 6

APPROVED	O.G. FIG.
BY	CLASS
DRAFTSMAN	SUBCLASS

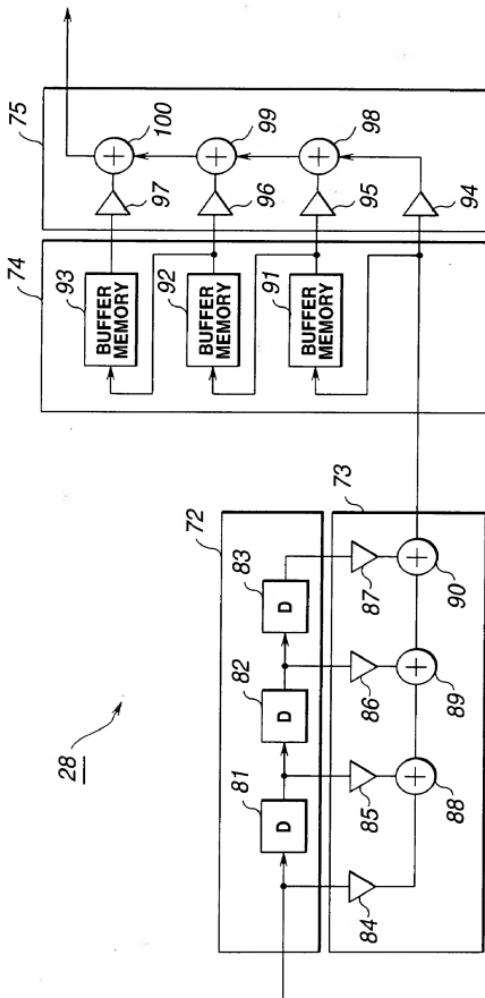


FIG.7

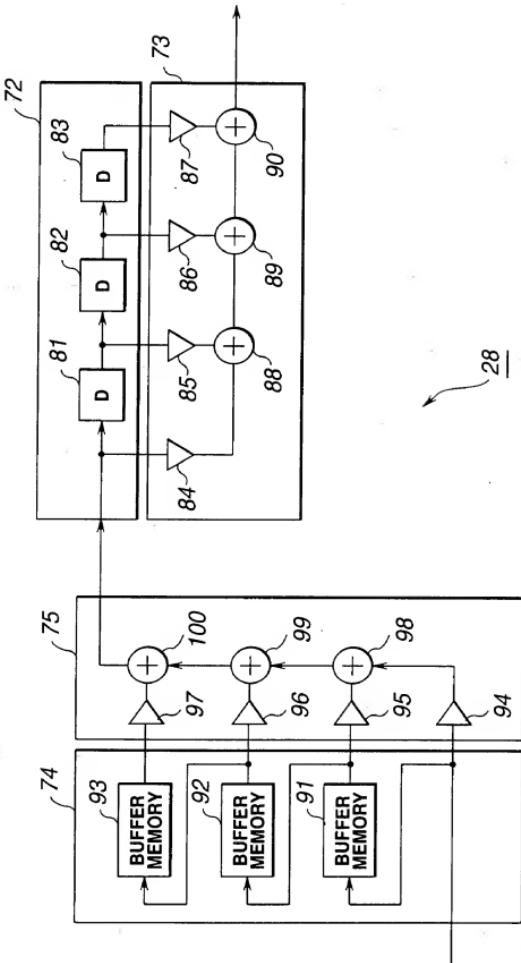


FIG.8

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

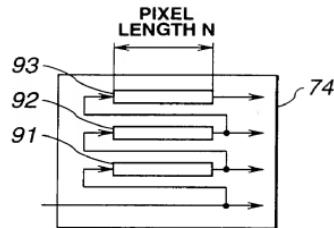


FIG.9

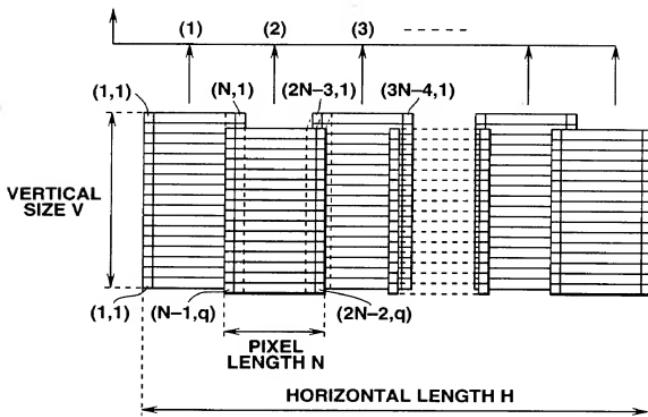


FIG.10

APPROVED BY DRAFTSMAN	O.G. FIG..
	CLASS SUBCLASS

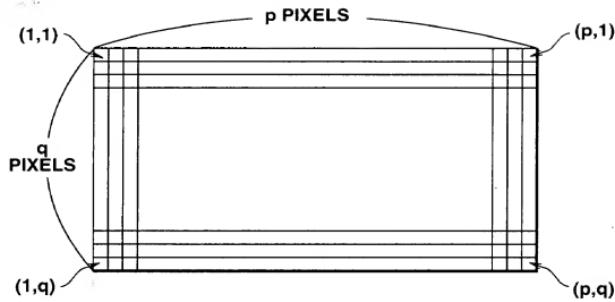


FIG.11

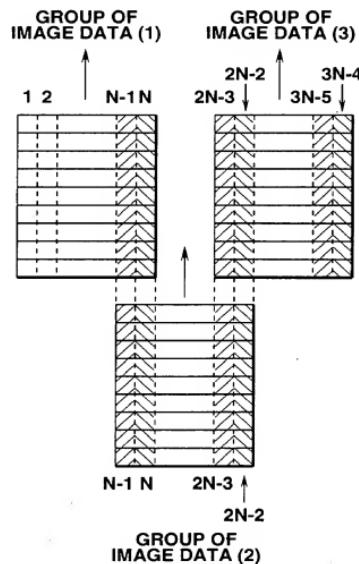


FIG.12

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

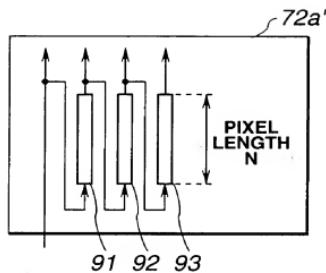


FIG.13

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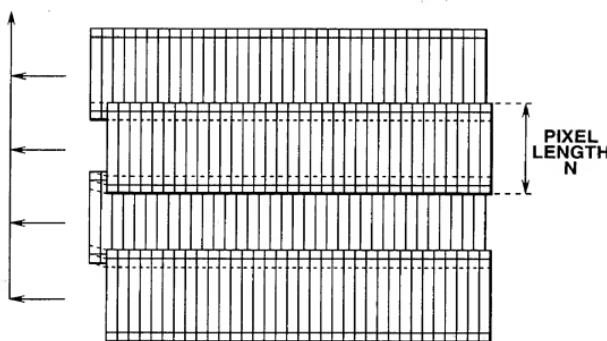


FIG.14

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

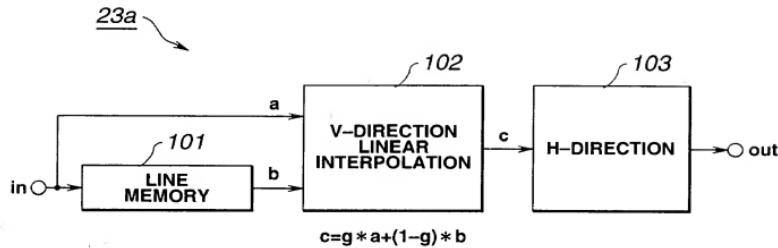


FIG.15

APPROVED BY DRAFTSMAN	O.G. FIG. CLASS	SUBCLASS
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FIG. 16A CCLK 12.27MHz

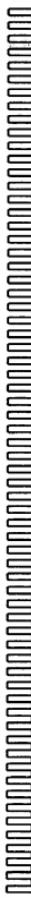
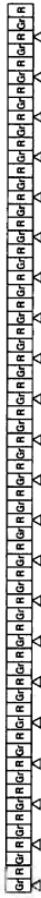


FIG. 16B CCD1F \rightarrow CAMDSP



1/3 THINNING

FIG. 16C CAMDSP →DRAM

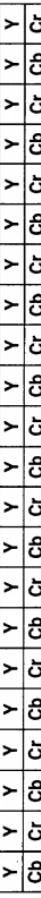
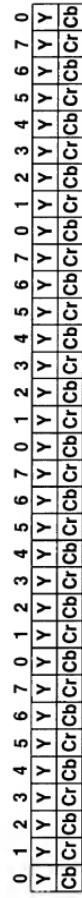


FIG. 16D DRAM→



YC-A22(320X240)

FIG. 16F ^{BUS→} DRAM (16bit)

